

# Separate Dual-Transistor Registers - A Circuit Solution for On-line Testing of Transient Error in UDSM-IC

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## Abstract

This paper addresses the soft-error problem in UDSM circuits by presenting on-line fault-tolerant circuit design techniques. In our scheme, separate dual transistor (SDT) structure is introduced into the register design as a key component to increase the input-signal stability as well as the robustness of the circuit against the effects of ionizing particles. Our work not only demonstrates the feasibility of its physical implementation, but also shows the cost effectiveness. To compare with other fault-tolerant techniques, ISCAS89 circuits have been synthesized with the SDT standard cells to investigate its cost/timing overheads. Our benchmark comparison reveals its better applicability over two representative techniques (TMR and ECC) for the logic circuits in digital systems.

## 1. Introduction

Electromagnetic (EM) noise sources such as crosstalk, transmission line effects and voltage drop collaborate to deteriorate signal integrity in Ultra-Deep-Submicron (UDSM) circuits [1]. With the shrinking of feature sizes, circuits themselves also become more sensitive to the various sources of interference [2][3]. These two facts imply that many factors, including numerous noise-coupling sources, manufacturing process variation and operation environments, can dynamically influence the functioning of circuit systems [4]. With increasing system complexity, it becomes difficult to predict such events and harder to prevent the consequent transient errors.

To address above problems, International technology Roadmap for Semiconductor (ITRS) predicts that fault-tolerant techniques like on-line error detection and correction will be the critical techniques for more reliable VLSI circuits with the technologies below 90 nm node [5]. In the past few years, several on-line fault-tolerant techniques have been developed for transient errors caused by EM interference and the effects of ionizing particles. Among them, circuit hardening, Triple Modular Redundancy (TMR) [2], and Error Correction Code (ECC) methods [6][7] are the most commonly used ones. TMR and ECC represent two different types of fault tolerant solutions exploiting space and time redundancy, respectively.

Circuit hardening techniques, which fall between them, has been intensively studied in the past few years and many techniques been proposed [8][9][10][11]. With

those methods, however, several issues still remain. First, latch itself is still a vulnerable but critical component. Thus, it needs extra hardening protection against particle strikes. A tighter design of sequential components might be achieved by introducing transistor duplication into sequential components. Also, little attention has been paid for the emerging topological effect of particle strike on UDSM circuits [9][12]. With the continual shrinking of circuit geometry, this effect is expected to be more important and the traditional hardening techniques might be less effective. A robust design may mandate an elaborated physical implementation against this effect in UDSM logic circuits. Further, the pros and cons of the circuit hardening techniques over other fault tolerant techniques have not been systematically studied before.

In this work, to address above issues, we present an elaborated design technique for sequential logic. The technique proposed in this paper provides a robust alternative to on-line repairing techniques of transient errors in digital circuits. The paper is organized as follows. Section 2 briefly describes the models and simulation methods for major transient errors. Section 3 presents the principle, schematic and layout designs of our SDT circuit. Section 4 shows the merits of this technique by a cost-performance analysis of benchmark circuits synthesized using SDT cells compared with TMR and ECC techniques. Finally, Section 5 concludes this work.

## 2 Transient Fault and Error Modeling

EM noise and ionizing particle strike are the two major sources of transient errors in UDSM circuit system [2]. It is essential to understand and model their behavior in order to facilitate fault tolerant designing process. For this purpose, we describe the EM and particle strike induced error effects separately as follows.

(1) For EM transient errors, the physical reasons are complex and usually the noise source is obscure. In a complex on-chip system, capacitive coupling, inductive coupling, inductive reflection, ground bounce, and substrate coupling can directly or partially contribute to a transient error. Once noise is generated somewhere in the circuit, it propagates through combinational logic to sequential logic or a primary output. If the arrival time of noise meets the sampling time window of sequential logic, an erroneous logic decision might be made and a stable erroneous signal generated at the output of the sequential element. We define this stable erroneous signal as *an error*. To determine the inputs that enable error conditions,

a worst-case analysis is usually performed. However, for large circuits, such analysis is expensive even for a single noise source such as IR drops [13]. The error conditions for such events are dynamic and non-deterministic.

To model such erroneous effects, we use a square-shaped glitch to represent the noise waveform. The occurrence probability of such a fault spreads over the entire clock cycle. The duration of the glitch is set to envelop the maximum EM noise duration in the combinational logic. An error occurs if it falls within the sampling time window of the receiving sequential logic. We define this fault model as *transient glitch fault model* in this paper.

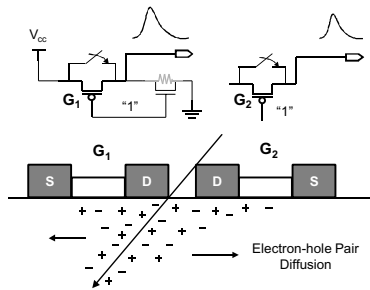


Figure 1. Particle strike on CMOS circuit and its size effect on DSM circuits.

(2) For particle-strike soft errors (known as single event upset or SEU), it is caused by temporary ionization effect of particle strike tracks in the transistor. Figure 1 illustrates the temporary transistor short effect of a radioactive particle penetrating through one CMOS inverter circuit. In Figure 1, G1 is a p-MOS gate of one CMOS inverter, and G2 is also a p-MOS gate adjacent to G1. As the input of the inverter is 1 (logic high), G1 is in OFF state. However, as the particle strikes through the inverter (as shown in Figure 1), the energy transferred from the particle track to G1 channels generates abundant electron-hole pairs. If the resulting carrier density is high enough, the transistor channel will be briefly shorted before they either drift away or combine with each other. Consequently, a pulse signal is generated on the output of the inverter. Usually such pulses have duration of several hundred pico-seconds and are considered to be hazardous.

In this paper, we use *temporary transistor short model* to describe the above behavior. In the temporary transistor short model, the effect can be simulated with the particle-stricken transistor in parallel with a switch. The OFF and ON switch states represent the normal and particle strike states. The ON duration is the lifetime of the ionized electron-hole pairs.

Further, if the geometry of the circuits is small enough, the ionized region, of which the affected area is dependent of the particle's incident angle, might affect G2 as the carriers diffuse into G2's channel. As a result, G2 might also be shorted and a spurious glitch generated at its output. We call this effect as *size effect* of particle strikes because it is related to the size of the circuit.

If the resulting glitch meets certain conditions, erroneous logic decision might be made at sequential logic or primary outputs. For particle strike induced errors, depending on where the particle strike hits, two different kinds of upset events may occur: (1) upsets generated inside the sequential components, and (2) upsets generated from the inputs of sequential components.

From above analysis, we know that transient fault modeling can be divided into two categories in terms of their different physical natures. One is the interference that comes from combinational logic, which can be modeled by an abstract transient glitch fault; the other is a temporary transistor short inside the sequential logic, which can be modeled by shorting drain and source nodes of the particle-stricken transistor, or our temporary transistor short model. In order to evaluate the robustness of a circuit to EM or particle-strike induced transient noise errors, we need to apply both models for a complete circuit simulation.

In the next section, we propose a circuit design technique that makes the hardened circuit insensitive to the glitch transient faults as well as the sequential transient faults. We use the above fault and error models to simulate circuits for design validation.

### 3 Proposed Scheme

A new scheme is proposed to harden the sequential logic in order to improve the robustness of the entire circuits with respect to the glitch transient faults from the combinational logic, as well as the sequential transient faults inside the sequential logic. The basic principle of this method is to use separate dual transistors (SDT). In this section, we first explain the operation of a latch cell with the SDT structure; and then show how this technique can be applied to harden D-type flip-flops (DFFs). Based on the transient faults developed in above section, we validate the SDT-enhanced standard cell designs with circuit-level fault simulation.

#### 3.1. SDT latch design

A traditional latch has a feedback loop that consists of two inverters. Figure 2 shows the schematic of one ordinary latch structure. In this figure, M1, M2, M3 and M4 are the four transistors on the inverter feedback loops. G1 and G2 are transmission gates controlled by clock signal. Note that: (1) This structure is vulnerable to the particle strike on the transistors M1, M2, M3 or M4. For example, if M3 is OFF and hit by one particle, the OFF channel will be shorted and the output logic at node Y turn to be logic 1 for several hundred pico-seconds. If the time is long enough, the output (logic 1) then puts M1 and M2 to the opposite states and the logic state of the latch experiences upset through the feedback loop. (2) The structure is also sensitive to the glitch transient faults. For example, if the input is a rising glitch and its arrival time is at the moment of the falling clock edge, the rising glitch may turn the output to be stable logic 1 in the rest of the clock cycle.

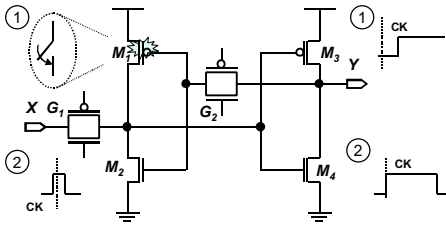


Figure 2. Standard static latch, its vulnerability to two types of faults. (1) transient transistor short inside the cell, and (2) incoming transient glitch.

To overcome these two hazards, a separated dual transistor structure (SDT) is introduced. The schematic of a SDT latch is shown in Figure 3. The dual transistor pairs in the schematic are (M1, M2), (M3, M4), (M5, M6) and (M7, M8). In this scheme, two signals D1 and D2 derived from the same inputs are applied to the latch: D1 is the incoming signal and D2 a delayed version of D1. The delay value is chosen to be longer than the summation of the setup time and duration of the glitch fault to ensure that at least one input is correct.

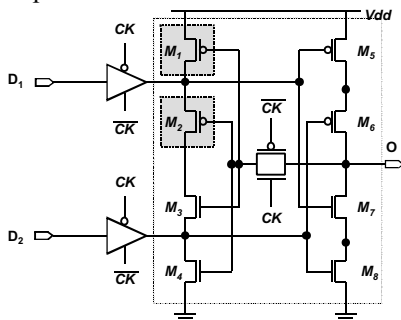


Figure 3. SDT latch schematic.

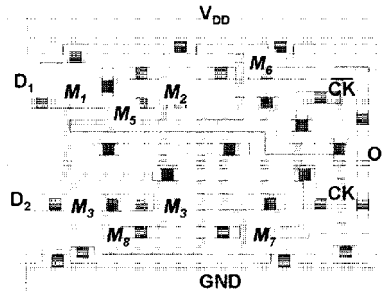


Figure 4. SDT latch layout.

Under normal operation, as the two signals D1 and D2 have the same logic value, the dual transistor pairs of output inverters (M5, M6) and (M7, M8) have the same values and pass the value to the output. However, if one of the signals is erroneous, the transistor pairs will have different states ( $S_{M5} \neq S_{M6}$  and  $S_{M7} \neq S_{M8}$ , where  $S_{M5}$ ,  $S_{M6}$ ,  $S_{M7}$ , and  $S_{M8}$  are the states of M5, M6, M7 and M8, respectively). Consequently, the paths from  $V_{dd}$  to O and O to GND are cut off and previous output value (or charge) is

locked at the output node Q in the latch until the signals become the same again. Because the delay is set to be larger than the sum of the glitch duration and set-up time, this latch is robust to the transient glitch at its inputs.

As shown in Figure 4, the latch can be implemented in an elaborated way that makes itself also immune to the effects of ionizing particles. In SDT structure, if one OFF transistor is shorted by a particle strike, the previous state will be kept in the latch as long as its twin transistor remains OFF. In this scheme, in order to tolerate the errors from the ionized area that might affect two adjacent transistor channels, the dual transistor pairs should be placed on different regions of the latch. For example, as a particle hits transistor M1 (assumed to be OFF), the channel of M1 will get shorted. As we explained in the last paragraph, dual transistor structure helps the latch to lock the logic states in such events. However, as the geometry of the transistor becomes comparable with the area ionized by particle strike, the channel of its twin transistor M2 may also collect the electron-hole pairs diffusing from M1 if they are geographically together, causing a short path from  $V_{dd}$  to 0. Thus, in the layout, M1 and M2 should be separated by M5 or M6, of which the channels are in ON state. In this way, the latch itself is robust to the size effect of particle strikes.

### 3.2 Layout implementation and design validation of a D-type flip-flop

D-type flip-flop (DFF) is an important component of sequential logic, consisting of a master-slave pair of latches. The clock sequence for the two latches is designed in such a way that as the master latch holds the data, the slave latch is transparent, and vice versa. In our design, the master and slave latches are SDT-based structure with the wiring connection shown in Figure 5. The delay value is set to be larger than the sum of glitch fault duration and the setup time of latch. In this configuration, the first latch is robust to both the glitch fault and the particle strikes on the internal transistors. Also, the second latch is immune to the particle strikes.

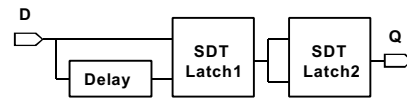


Figure 5. SDT DFF schematic.

We implemented the layout of SDT DFF using  $0.18 \mu\text{m}$  technology. The cell size is  $5.4 \mu\text{m} \times 23.03 \mu\text{m}$ , whereas the one of the normal DFF in our standard cell library is  $5.4 \mu\text{m} \times 14.52 \mu\text{m}$ . In our design, as shown in Figure 6, a standard buffer cell consisting of four inverters is placed next to the inputs of SDT latch. The delay can range from 100 ps to 500 ps, depending upon the design of MOS gate length of the inverters. The area overhead of our DFF cell is about 58.6 %. Note that the delay cell size is set to be a fixed value so that its size is independent of the

delay value as the delay is below 600 ps. We have also calibrated the cell timing characteristics of the new cell using post-layout circuit simulation. The comparison data are listed in Table 1.

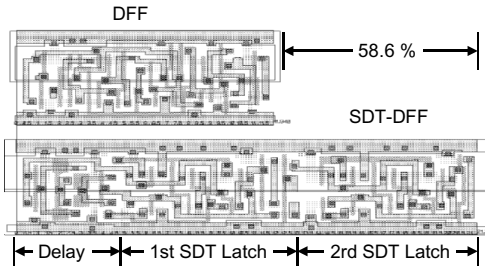


Figure 6. Layouts of standard DFF and SDT DFF.

Table 1. Comparison of standard DFF and SDT-DFF.

	Standard DFF	SDT-DFF
Area ( $\mu\text{m}^2$ )	5.4 x 14.52	5.4 x 23.03
$t_{\text{rise}}$ (ps)	155	241
$t_{\text{fall}}$ (ps)	205	211

We performed circuit-level fault simulation to evaluate the robustness of our design. For the glitch fault in this experiment (300 ps), the faults were randomly inserted to the input signals of normal DFF and SDT-DFF cells. To evaluate immunity against the particle strikes, we used a switch model to simulate the shorting behavior of ionizing particles in transistor channels. Our SPICE simulation results show that the SDT circuits endure both glitch transient faults as well as temporary transistor short faults.

#### 4. Comparison Study

We have evaluated the applicability of the proposed scheme for generic circuits in terms of performance and area overhead. In our experiment, the ISCAS89 benchmark have been mapped into EDIF-formatted circuit netlists with 0.18  $\mu\text{m}$  standard cells, and subsequently the EDIF format netlist compiled to generate a synthesizable Verilog netlist by Synopsys synthesis tool (Design Compiler). Last the Verilog designs were implemented into layout with Cadence placement and routing tool (Silicon Ensemble DSM). The timing analysis and area cost were investigated from this logic-to-layout synthesis process.

Table 2 and Table 3 list our timing and area overhead results. In this experiment, the delay time is set to be 343 ps. As shown in Table 2, the maximal critical path timing increase is 17.8 % for s526 and the minimal one 7.5 % for s1196. The timing overhead varies from 7.5 % to 17.8 %, depending on the maximum number of levels in the circuits. The average timing overhead from our benchmark study is 10 % in this case (343 ps delay). For the area overhead, the hardware cost ranges from 5.9 % to 11.8 %, depending on the contribution of DFF number to the area of the circuits.

Figure 7 and Figure 8 show the comparison of timing and area overheads of three different techniques-

TMR, ECC and our SDT-based scheme. The TMR and ECC data are from [6]. Note that the technology we used here is different from theirs. However, since the benchmark circuits used in the papers are the same, the overhead percentage across different technologies should not vary significantly.

Table 2. Timing overhead of ISCAS 89 Benchmark circuits.

Ckt #	DFF#	Gate#	$CP_0$ (ns)	$CP^*$ (ns)	TOH* (%)
S526	21	193	1.69	2.04	17.8
S641	19	379	5.14	5.49	5.87
S713	19	393	5.40	5.74	5.6
S838	32	446	2.54	2.86	11.8
S953	29	395	1.95	2.30	15.4
S1196	18	529	2.71	3.05	11.0
S1238	18	508	2.88	3.23	10.4
S1423	74	657	8.78	9.16	3.4
S5378	179	2779	2.69	3.26	11.2

\* $CP_0$  and  $CP^*$ : critical path without/with SDT structure

\*TOH: timing overhead

\*delay time: 343 ps

Table 3. Area overhead of ISCAS89 Benchmark circuits.

Ckt #	DFF#	Gate#	Area <sub>0</sub> ( $\mu\text{m}^2$ )	Area ( $\mu\text{m}^2$ )	AOH* (%)
S526	21	193	8633	9549	15
S641	19	379	10853	11722	10.8
S713	19	393	11269	12088	10.4
S838	32	446	13962	15210	14.2
S953	29	395	12010	13413	14.9
S1196	18	529	14762	15433	7.5
S1238	18	508	14702	15473	7.6
S1423	74	657	23868	26948	19.2
S5378	179	2779	80277	87838	13.8

\*Area<sub>0</sub> and Area: area without/with SDT structure

\*AOH: area overhead

Because the timing overhead of our technique is dependent of the delay value in SDT-DFF design (higher delay means more robust but less performance), 300 ps and 600 ps delays are used for two SDT-DFF standard cells to determine the cost in this experiment. As shown in Figure 7, as the delay is about 300 ps, the timing overhead of our technique is always lower than the other two techniques. As the delay rises to 600 ps, the timing overhead becomes comparable with TMR (around 20 % in average) but still much smaller than ECC.

For the area overhead, our technique shows much better results than both TMR and ECC. From Figure 8, the average area overhead of ECC and TMR are found to be around 106 % while our scheme just 13 %. Our comparison study clearly shows better cost-effectiveness of the sequential circuit hardening techniques over ECC and TMR.

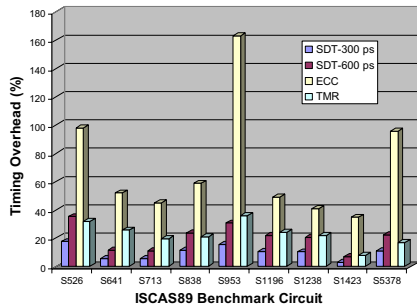


Figure 7. Timing overhead comparison between SDT, TMR and ECC techniques.

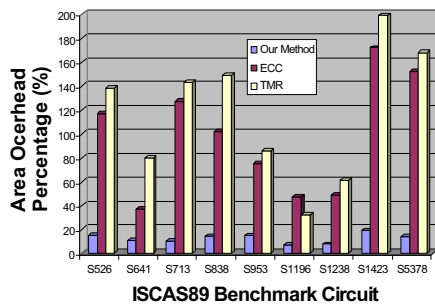


Figure 8. Area overhead comparison between SDT circuit, TMR and ECC techniques.

In fact, ECC hardens the circuit in the unit of redundant informative bit. As a high-level fault-tolerant technique, one of its merits is that it can tolerate a wide range of transient errors in the system, though the redundancy cost might be high. For the circuits like memory, where the micro-architecture is highly symmetric, this method turns out to be effective. However, for generic logic, as shown in our experiment, the redundant bits may lead to high cost in terms of either timing or area cost.

For TMR, the method triplicates the key parts of the circuits and thereby always has significant high area cost. In conventional circuit, the timing overhead imposed by voting circuit is always low. In UDSM circuit, however, due to the decreasing depth of pipeline in sequential circuit, the timing overhead of this part will increase.

Compared with above two techniques, hardening sequential cells introduce time and area redundancy in the unit of hazardous noise width or transistor. Therefore, in nature, it is a more elaborated solution for transient errors induced by particle strike and short-life crosstalk noise, as long as the fault model is valid. As a result, the timing and area overheads of this technique are more cost effective than the other two peer techniques.

## 5. Conclusions

In conclusion, a circuit hardening technique is proposed to improve the reliability of UDSM integrated

circuits against transient errors generated by EM noise and particle strikes. In our design, separate dual transistor (SDT) structure is developed for sequential logic components. Our experiments confirm that the SDT-DFF cells are robust to the glitch noise as well as particle-strikes on the cells. We also compared its cost-effectiveness with TMR and ECC methods as we hardened ISCAS89 benchmark circuits with our technique. The average performance involved with our scheme is moderate (10-20 %, depending on delay redundancy configuration) whereas the area cost is as low as 13 %. Our comparison study suggests that as a more elaborated solution, the SDT hardening technique is superior to TMR and ECC in terms of area and performance cost. This result clearly indicates SDT latch design as one promising alternative for more reliable VLSI circuits under 90 nm node. In our future work, SDT circuit fabrication and its ground radiation test will be conducted for further investigation.

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